CS46

USN

NEW SCHEME

Fourth Semester B.E. Degree Examination, Dec. 06 / Jan. 07
CS / IS / EC / TE / EE / IT / ML / BM
Computer Organisation

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Briefly explain the history of computer development from first generation to fourth generation computers. **(08 Marks)**

b. Quoting an example for each explain :
   i) Different types of instructions in a computer to perform various operations.
   ii) Different addressing modes used to specify the location of operand.
found in most computers. **(09 Marks)**

c. List three important differences between how a stack and a queue are organized. **(03 Marks)**

2 a. Convert the following pairs of decimal numbers to 5-bit, signed, 2's complement binary numbers and add them. State whether or not overflow occurs in each case.
   i) 7 and 13
   ii) –5 and 7
   iii) –14 and 11
   iv) –10 and -13 **(08 Marks)**

b. With the help of suitable examples, illustrate encoding of machine instructions. **(12 Marks)**

3 a. For a simple example of I/O operations involving a keyboard and a display device, write a assembly language program that reads one line from the keyboard, stores it in memory buffer and echoes it back to the display. **(08 Marks)**

b. In a situation where number of operationally independent devices capable of initiating interrupts are connected to a processor, what are the different challenges faced by the processor? How does the processor take care of these challenges? **(12 Marks)**

4 a. Showing the possible register configurations in a DMA interface, explain direct memory access. **(08 Marks)**

b. Considering the timing diagrams, explain the sequence of events for input transfer and output transfer on a synchronous bus. **(08 Marks)**

c. List out the functions of an I/O interface. **(04 Marks)**

5 a. With the block diagram explain the operation of a 16-megabit DRAM chip configured as 2M×8.

b. Which are the various factors to be considered in the choice of a memory chip? Explain.

c. Give the organization of a 2M×32 memory module using 512k×8 static memory chips.

... a block on flash memory.

b. Is the average access time experienced by the processor an excellent indicator of the effectiveness of a particular implementation of the memory hierarchy? Explain. **(06 Marks)**

c. With a block diagram explain the virtual memory organization. **(08 Marks)**

7 a. A half adder is a combinational logic circuit that has two inputs, x and y and two outputs, s and c, that are the sum and carry-out respectively, resulting from the binary addition of x and y.

i) Design a half adder as a two-level AND-OR circuit.

ii) Show how to implement a full-adder using two half-adder and external logic gates as necessary.

iii) Compare the longest logic delay path through the network derived in part (ii) to that of the logic delay of the adder network implemented using basic gates. **(06 Marks)**

b. Illustrate with an example the algorithm for non restoring binary division. **(05 Marks)**

c. Write IEEE standard floating-point formats for 32-bit representation and explain. **(08 Marks)**

8 a. With the control sequence for the instruction add R_4, R_5, R_6, explain the three-bus organization of data path in a processor. **(07 Marks)**

b. Explain microinstruction sequencing with next address field. **(08 Marks)**

c. Explain the example of embedded system in a digital camera. **(06 Marks)**